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10CS33

Third Semester B.E. Degree Examination, June/July 2018
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define (i) period, (ii) frequency and (iii) duty cycle of a digital signal. The waveform has a frequency of 5 MHz and width of positive pulse is 0.05 μs. What is the high duty cycle and low duty cycle? **(06 Marks)**

b. What are universal gates? Realize the basic gates using NOR gates only. **(04 Marks)**

c. What is the purpose of using an expander, with an AND-OR-INVERT gate? Write a logic circuit of an expander driving expandable AND-OR-INVERT gate. **(05 Marks)**

d. What are the three different models for writing a module body in verilog HDL? Explain the structure of verilog module. **(05 Marks)**

2 a. Use k-map to simplify the following Boolean expression and give the implementation of the same using NOR gates only (pos form):

$F(A, B, C, D) = \Sigma m(0, 1, 2, 4, 5, 12, 14) + d(8, 10)$ **(08 Marks)**

b. Simplify the following Boolean expression using Quine-Meclusky method

$F(A, B, C, D) = \Sigma m(1, 2, 8, 9, 10, 12, 13, 14)$ **(08 Marks)**

c. What are static hazards? Explain with an example to design a hazard free circuit. **(04 Marks)**

3 a. Implement the following Boolean expression using a 4:1 multiplexer and external gates, Take 'AB' as input to multiplexer selection lines and CD as map entered variables (input variables).

$F(A, B, C, D) = \Sigma m(6, 7, 9, 10, 13) + d(1, 4, 5, 11)$ **(06 Marks)**

b. Implement the following Boolean functions using PLA:

$f_1(a, b, c) = \Sigma m(0, 1, 3, 4)$

$f_2(a, b, c) = \Sigma m(1, 2, 3, 4, 5)$ **(06 Marks)**

c. Design a 1-bit comparator. **(04 Marks)**

d. Write a verilog module for 2:1 multiplexer using if else statement and case statement. **(04 Marks)**

4 a. What is Race around condition? How do you overcome this problem? **(06 Marks)**

b. Show how a D-flip flop can be converted to SRFF. **(06 Marks)**

c. Analyze the behavior of the sequential circuit shown in Fig.Q4(c) and draw the state table and state transition diagram. **(08 Marks)**

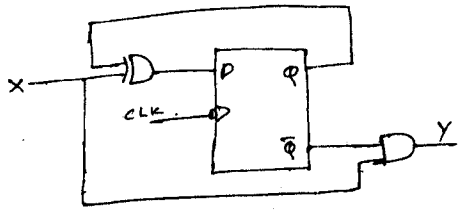

Fig.Q4(c)

PART – B

5 a. Explain the different types of shift registers and also explain how the shift registers can be used for counting applications. **(10 Marks)**

b. Discuss with a neat diagram, how the shift register can be used for Serial Addition. **(06 Marks)**

c. Explain with an example, the difference between Blocking assignment statements (=) and non Blocking assignment statements (<=). **(04 Marks)**

6 a. Mention any two differences between asynchronous and synchronous counter, with a neat block diagram, output waveforms and truth table, explain a 3-bit ripple down counter constructed using negative-edge triggered JK flip-flops. **(10 Marks)**

b. Design a self correcting modulo-6 synchronous counter using JK flip-flop as described in state sequence of Fig.Q6(b), in which all the unused state leads to state CBA = 000.

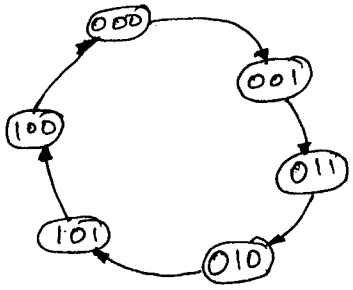

Fig.Q6(b) **(10 Marks)**

7 a. Compare Moore and Mealy model of synchronous sequential circuit. **(05 Marks)**

b. Draw the ASM chart for vending machine problem using Mealy model. **(05 Marks)**

c. Reduce the state transition diagram of Fig.Q7(c) by
(i) Row elimination method (ii) Implication Table method. **(10 Marks)**

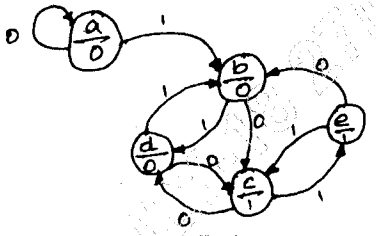

Fig.Q7(c)

8 a. What is Binary ladder? Explain the binary ladder with a digital input of 1000. **(06 Marks)**

b. Discuss the working of the following A/D converters:
(i) 3 - bit simultaneous A/D converter
(ii) Continuous A/D converter. **(10 Marks)**

c. A counter type 8-bit A/D converter driven by a 500 kHz clock, find
(i) The average conversion time
(ii) The maximum conversion rate. **(04 Marks)**

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